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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/707,625	ENGLIN ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 5, 11, and 18 are objected to because of the following informalities:

Referring to line 2 of claim 5, the "stored tag address with the memory address access" is understood to refer to "the corrected tag address with the memory access address", correcting for antecedent errors.

Referring to the last lines of claims 11 and 18, Applicant has claimed "a current address", wherein a current address can refer to the "addresses currently cached", rendering "a current address" an unclear, if intended, antecedent. From the specification, Examiner understands that the second address compare module compares, instead, the "requested address".

Appropriate correction is required. Examiner notes that this is the **second** time these objections have been made.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-3, 5-7, 11, 12, 14, 15, 17-20, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5509119 to La Fetra. Referring to claim 1, La Fetra discloses retrieving a stored tag address from the tag memory in response to the requester submitting a memory access address (From line 57 of column 3, " In operation, the CPU address Tag 201 is asserted by a CPU. The CPU-Tag is fed into the Tag input 207 of the comparator and simultaneously fed into the index input 203 of the cache RAM 205. The index input is the address input of the cache RAM. The

cache RAM then outputs the Cache-Tag and the ECC information 213 associated with the memory location in the cache RAM addressed by the index input. In this example, Cache-Tag 211 and its associated ECC 213 are presented on the outputs of the cache RAM and fed into the inputs 217 and 219 respectively of the Tag check and correct circuit 215."); performing a first comparison of the memory access address to the stored tag address, without regard to any error correction code associated with the stored tag address, to determine whether the requested data is stored in the cache memory (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)." Wherein the second comparator 401 disclosed by La Fetra is comprised of two comparisons, the Cache-Tag/CPU-Tag comparison and the Cache-ECC/CPU-ECC

comparison. Further, from line 32 of column 4, "Given an address asserted by the CPU (CPU-Tag), the information that must be in the cache entry 101 for a cache hit to occur is predictable. That is, the Cache-Tag must match the CPU-Tag."); monitoring for errors in the stored tag address contemporaneously with the first comparison of the memory access address and the stored tag address (From line 1 of column 4, "The Tag check and correct circuit 215 checks the Cache-Tag for errors using the ECC information and corrects the Cache-Tag if an error is found. This checked and corrected Tag is then presented on the output 221 of the circuit and fed to the corrected Tag input 223 of the Tag comparator 209. After the corrected Tag is available to the Tag comparator 209, the comparator compares the corrected Tag to the CPU-Tag and if the two Tags match, the comparator outputs a true hit signal on output line 225. This signal is used by the cache memory system to provide data in the cache memory to the CPU by methods known in the art. If the two Tags do not match, then there has been a cache miss and the cache is updated as previously discussed."); if a tag address error is detected in the stored tag address, disregarding the first comparison, correcting the tag address error, and performing a second comparison of the memory access address and the corrected tag address to determine whether the requested data is stored in the cache memory (From line 25 column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."); and if no tag address error is detected in the stored tag address, utilizing results of the first comparison to determine whether the requested data is stored in the cache memory (From line 22 column 5, "Since, most of the time the cache

tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow.").

Referring to claim 2, La Fetra discloses monitoring for errors in the stored tag address comprises identifying at least one error using a single error correction code associated with the stored tag address in the tag memory (From figure 2, element 205. Further, from line 66 of column 4, "The cache RAM 205, Tag check and correct circuit 215 and the Tag comparator 225 function as discussed in association with FIG. 2 and provide the same true hit output 225 as before.").

Referring to claim 3, La Fetra discloses the single error correction code is coded to provide error detection for the stored tag address and a plurality of configuration fields (From line 40 of column 3, "FIG. 1 illustrates a typical cache Tag-ECC entry 101 having three primary segments 103, 105 and 107. Segment 105 contains "house keeping" information such as bits that indicate the cache is "dirty" or "private". The ECC field 107 has error correcting data for both the Tag segment 103 and the house keeping segment 105.").

Referring to claim 5, La Fetra discloses the second comparison compares only the requested tag address with the memory access address, and disregards comparison of any stored error correction code bits (From line 1 of column 4, "The Tag check and correct circuit 215 checks the Cache-Tag for errors using the ECC information and corrects the Cache-Tag if an error is found. This checked and corrected Tag is then presented on the output 221 of the circuit and fed to the corrected

Tag input 223 of the Tag comparator 209. After the corrected Tag is available to the Tag comparator 209, the comparator compares the corrected Tag to the CPU-Tag and if the two Tags match, the comparator outputs a true hit signal on output line 225.").

Referring to claim 6, La Fetra discloses performing the first comparison and monitoring for errors in the stored tag address occur contemporaneously with correcting the tag address error and performing the second comparison (From figure 4, the Fast Hit 407 and True Hit 225 are shown to operate in parallel. Further, from line 16 of column 25, "Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns). Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow. If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.").

Referring to claim 7, La Fetra discloses correcting the tag address error and performing the second comparison are initiated upon recognition of a tag address error (From line 1 of column 4, "The Tag check and correct circuit 215 checks the Cache-Tag for errors using the ECC information and corrects the Cache-Tag if an error is found. This checked and corrected Tag is then presented on the output 221 of the circuit and fed to the corrected Tag input 223 of the Tag comparator 209. After the corrected Tag is available to the Tag comparator 209, the comparator compares the corrected Tag to

the CPU-Tag and if the two Tags match, the comparator outputs a true hit signal on output line 225.").

Referring to claim 11, La Fetra discloses a cache hit detector, comprising: (a) a tag memory to store tag addresses corresponding to addresses currently cached (From figure 4, element 205); (b) a fast hit detection circuit, comprising: (i) a first address compare module coupled to the tag memory to receive a tag address and to compare the tag address to a requested address (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)."); (ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address (From line 2 of column 5, "A second comparator 401 is provided which

receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)."); (iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if and only if no error is discovered by the error detector and the requested address is stored in the tag memory (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-

Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407." Further, line 25 of column, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."); (c) a slow hit detection circuit, comprising: (i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address (From figure 4, element 215.); and (ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare the corrected tag address to the requested address (From figure 4, element 209.).

Referring to claim 12, La Fetra discloses the fast hit detection circuit and the slow hit detection circuit are coupled in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit (From figure 4, the Fast Hit 407 and True Hit 225 are shown to operate in parallel. Further, from line 16 of column 25, "Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns). Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow.

If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.").

Referring to claim 14, La Fetra discloses the tag memory further stores an error correction code for each block of data stored in the tag memory, wherein each block of data is associated with a single error correction code, and the single error correction code provides error correction capabilities for the stored tag address and a plurality of configuration fields (From line 40 of column 3, "FIG. 1 illustrates a typical cache Tag-ECC entry 101 having three primary segments 103, 105 and 107. Segment 105 contains "house keeping" information such as bits that indicate the cache is "dirty" or "private". The ECC field 107 has error correcting data for both the Tag segment 103 and the house keeping segment 105.").

Referring to claim 15, La Fetra discloses the first address compare module and the error detector are coupled in parallel to contemporaneously compare the tag address to a requested address and determine whether there are any errors in the tag address (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the

Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)." Wherein the second comparator 401 disclosed by La Fetra is comprised of two comparisons, the Cache-Tag/CPU-Tag comparison and the Cache-ECC/CPU-ECC comparison.).

Referring to claim 17, La Fetra discloses the error detector determines whether there are any single bit errors in the tag address (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through

the Tag check and correction circuit 215 (approximately 2 ns)." Wherein any comparison that is not equal constitutes at least a single bit error.).

Referring to claim 18, La Fetra discloses a data processing system comprising: (a) a main memory module for storing data (From line 14 of column 1, "a main memory".); (b) at least one cache memory coupled to the main memory module to cache at least a portion of the data stored in the main memory module (From line 20 of column 1, "a cache".); (c) at least one processing unit (From line 13 of column 1, "a central processing unit".) to process data and to control data access with the main memory module and the cache memory, the processing unit comprising: (1) a tag memory to store tag addresses corresponding to addresses currently cached (From figure 4, element 205.); (2) a fast hit detection circuit, comprising: (i) a first address compare module coupled to the tag memory to receive a tag address and to compare the tag address to a requested address (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401

outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)."); (ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407. Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns)."); (iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if and only if no error is discovered by the error detector and the requested address is stored in the tag memory (From line 2 of column 5, "A second comparator 401 is provided which receives

the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407." Further, line 25 of column, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."); (3) a slow hit detection circuit, comprising: (i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address (From figure 4, element 215.); and (ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare the corrected tag address to the requested address (From figure 4, element 209.).

Referring to claim 19, La Fetra discloses the fast hit detection circuit and the slow hit detection circuit are configured in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit (From figure 4, the Fast Hit 407 and True Hit 225 are shown to operate in parallel. Further, from line 16 of column

25, "Since the ECC generator derives the CPU-Tag ECC in parallel with the cache RAM access, the time required to assert the fast hit signal is less than required to assert the true hit signal by the delay time through the Tag check and correction circuit 215 (approximately 2 ns). Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow. If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.").

Referring to claim 20, La Fetra discloses the tag memory further stores an error correction code associated with each block of data, wherein each block of data is associated with a single error correction code, and the single error correction code! provides error correction capabilities for the stored tag address and a plurality of configuration fields (From line 40 of column 3, "FIG. 1 illustrates a typical cache Tag-ECC entry 101 having three primary segments 103, 105 and 107. Segment 105 contains "house keeping" information such as bits that indicate the cache is "dirty" or "private". The ECC field 107 has error correcting data for both the Tag segment 103 and the house keeping segment 105.").

Referring to claim 22, La Fetra discloses a cache hit detector, comprising: (a) means for storing tag memory addresses corresponding to addresses of data currently stored in cache memory (From figure 4, element 205.); (b) means for providing alternate cache hit detection via concurrent processing on each of at least two cache hit detection paths, the alternate cache hit detection means comprising: (1) first hit detection path

means for detecting cache hits without first performing error detection and correction (From figure 4, "Fast Hit" path 407.); (2) second hit detection path means for detecting cache hits, the second hit detection path means comprising: (i) means for detecting errors in the tag memory address (From figure 4, element 215.); (ii) means for correcting the tag memory address if errors in the tag memory address are discovered (From figure 4, element 215.); (iii) means for detecting for cache hits using the corrected tag memory address if errors in the tag memory address are discovered (From figure 4, element 209.); and (iv) means for disabling the first hit detection path means if errors in the tag memory address are discovered (From line 25 column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."); and (c) means for coordinating timing between the first hit detection path means and the second hit detection path means (From line 22 of column 5 (with emphasis), "Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow. If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system **waits** for the true hit/miss signal as before.").

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5509119 to La Fetra as applied to claim 1 above. Referring to claims 8 and 9, La Fetra discloses disregarding the first comparison results of the first comparison through an output gate (From line 25 column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."). Although La Fetra does not specifically disclose said disregarding comprises blocking passage of the results by providing an error signal to the result signal's output gate when a tag address error is detected and disabling an output of the output gate upon receipt of the error signal, blocking a signal on error is notoriously well known in the art. Examiner takes official notice for a logic gate. A person of ordinary skill in the art at the time of the invention would have been motivated to block a signal on error using a logic gate because, from line 25 of column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before." Wherein this being computer logic, a person of ordinary skill in the art at the time of the invention would have been motivated to pass the output through a "gate" of some kind, even if not explicitly disclosed as such, because a gate is an electronic switch that is the elementary component of a digital circuit that produces an electrical output signal that represents a binary 1 or 0 and is related to the states of one or more input signals by an operation of Boolean logic and La Fetra has disclosed that a tag error is detected (an input signal that represents a state) that results in the disallowance of a fast hit

assertion (an electrical output signal that represents a binary 1 or 0).

Referring to claim 10, La Fetra discloses enabling the tag address error to be corrected and the second comparison of the memory access and corrected tag addresses to be performed in response to the error signal (From line 22 column 5, "Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow.").

6. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5509119 to La Fetra as applied to claim 11 above, in further view of "Pipelined Datapath" from ***Logic and Computer Design Fundamentals*** by Mano et al. Referring to claim 13, La Fetra discloses means to coordinate timing between the fast hit detection circuit and the slow hit detection circuit (From line 25 column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before."). Although La Fetra does not specifically disclose latching as this means, storing for subsequent operation is notoriously well known in the art. An example of this is shown by Mano et al. on page 348. More specifically, referring to figure 7-23, it can be seen in the operand fetch stage, as an example, a register file read incurs a 3 ns delay and a mux selection incurs a 1 ns delay; registers between the stages store data for operation by the next stage. As can be seen from this first stage, there are two separate datapaths: one for A data and one for B data. A data does not have a mux selection and therefore does not incur an additional 1 ns delay, however, since the next stage in the pipeline cannot use the data

until both A data and B data are ready (and hence, a 4 ns total delay for that stage of the pipeline), that data is stored in the pipeline platform (registers, which are composed of latches, extremely basic elements of computer logic). Then in the next stage, when the data is ready, the data is read out and a function is applied to it. A person of ordinary skill in the art at the time of the invention would have been motivated to store a result for subsequent operation because, as was shown by Mano et al., there are unequal delays for the data prior to arriving at the operation (From line 5 of page 348, "as soon as all of the tasks in a particular stage are done, the conveyor belt can move forward so that the same tasks can be performed on the next items on the belt.") and so that a task may be broken down into stages (From line 8 of page 346, "we need to be concerned about the speed or rate at which the microoperations are performed." Further from paragraph 3 of page 347, "A conveyor belt moves components from stage to stage by proceeding forward periodically the length of one stage. Components and partially completed assemblies are stored in bins."). La Fetra would have been motivated to use latches to store a result for subsequent operation because signals arrive unequally (From line 25 of column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.") and memory access works in cycles.

Referring to claim 16, La Fetra discloses first address comparison results and a resulting error indicator signal (From line 2 of column 5, "A second comparator 401 is provided which receives the Cache-Tag / Cache-ECC pair from the cache RAM 205. Another input of the second comparator 401 receives the CPU address Tag 403 and a

derived CPU-Tag ECC generated by an ECC generator 405. The ECC generator 405 takes the CPU-Tag and computes the appropriate ECC for that Tag in the same manner as is used to derive the Cache-ECC stored in the cache memory. This ECC generator derives the CPU-Tag ECC in the same or less time than is required to access the Cache-Tag/Cache-ECC pair from the cache RAM. The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC."). Although La Fetra does not specifically disclose latching the comparison and error indicator signal, wherein the comparison results and the error indicator signal are not passed to the gated output until both the comparison results and the error indicator signal are available at the latches, and until simultaneously clocked to concurrently provide the comparison results and the error indicator signal to the gated output, storing for subsequent operation is notoriously well known in the art. An example of this is shown by Mano et al. on page 348. More specifically, referring to figure 7-23, it can be seen in the operand fetch stage, as an example, a register file read incurs a 3 ns delay and a mux selection incurs a 1 ns delay; registers between the stages store data for operation by the next stage. As can be seen from this first stage, there are two separate datapaths: one for A data and one for B data. A data does not have a mux selection and therefore does not incur an additional 1 ns delay, however, since the next stage in the pipeline cannot use the data until both A data and B data are ready (and hence, a 4 ns total delay for that stage of the pipeline), that data is stored in the pipeline platform (registers, which are composed of latches, extremely basic elements of computer logic). Then in the next stage, when the data is ready, the data is read out and

a function is applied to it. A person of ordinary skill in the art at the time of the invention would have been motivated to store a result for subsequent operation because, as was shown by Mano et al., there are unequal delays for the data prior to arriving at the operation (From line 5 of page 348, "as soon as all of the tasks in a particular stage are done, the conveyor belt can move forward so that the same tasks can be performed on the next items on the belt.") and so that a task may be broken down into stages (From line 8 of page 346, "we need to be concerned about the speed or rate at which the microoperations are performed." Further from paragraph 3 of page 347, "A conveyor belt moves components from stage to stage by proceeding forward periodically the length of one stage. Components and partially completed assemblies are stored in bins."). La Fetra would have been motivated to use latches to store a result for subsequent operation because signals arrive unequally (From line 25 of column 5, "If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.") and memory access works in cycles. Further, La Fetra would have been motivated to store for subsequent comparison and to gate a signal because, from line 15 of column 5, "If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407.", wherein La Fetra has clearly shown that the comparator 401 output is contingent upon both the Tag and ECC comparisons and a correct output cannot occur until both Tag and ECC comparisons have been generated.

Response to Arguments

7. Applicant's arguments filed 11 March 2004 have been fully considered but they are not persuasive. In response to Applicant's argument regarding claim 1 that La Fetra does not disclose comparing a tag address without regard to ECC, it is clear from Applicant's specification that applicant is speaking of the ECC bits that are stored. Applicant previously did not claim as broadly as "associated", however it is clear that this "associated" ECC is stored ECC bits. From the abstract, "A single error correction code (ECC) is used to minimize storage requirements, and data hit comparisons based on the cached address and requested address are performed exclusive of ECC bits to minimize bit comparison requirements." Further, from line 4 of page 3 of Application's specification, "Prior art systems have also utilized multiple error correction codes, requiring additional memory capacity to house all of the ECC information. Further, these prior art systems perform a comparison of all bits, including ECC bits, which adversely affects performance." From line 8 of page 4 of Applicant's specification, "The present invention utilizes a single error correction code (ECC), to minimize storage requirements, and performs "hit" comparisons based on the cached address and requested address, exclusive of ECC bits, so that fewer bits are compared and performance is increased." From line 14 of page 21 of the Applicant's specification, "The single ECC code 600 includes a plurality of ECC bits forming a code corresponding to the bit sequence of the data, which is then stored along with the data. The ECC code 600 is formed from the plurality of data fields, including the stored address 602, the valid field 604, the ownership field 606 and the written field 608. A preferred embodiment of the invention uses only one ECC code for all of the data fields, so that fewer ECC bits

need to be stored in the memory, thereby reducing the requisite size of memory. However, in performing the fast hit address compare in accordance with one embodiment of the invention, only the stored address in field 602 is compared to the address presented by the processor (i.e., the "set address"), and no comparison of ECC bits is performed."

Further, as stated in the previous office action, the second comparator 401 is comprised of **two** comparisons, in which the Cache-tag/CPU-tag is compared and the Cache-ECC/CPU-ECC is compared. From line 13 of column 5 (with emphasis), "The second comparator 401 compares the Cache-Tag to the CPU-Tag **and** compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407." It is only upon both of these **separate** comparisons being performed that a fast hit is generated. Regardless of the comparison of ECC data, the tag comparison occurs. It is the outcome of both of these separate comparisons that determines whether or not a fast hit occurs.

In response to Applicant's argument that any error monitoring that is performed contemporaneously with La Fetra's fast hit path is used only in the path leading to the True Hit 225, Examiner disagrees. Examiner has cited previously, and herein cites again, that La Fetra performs error detection/monitoring in the fast hit path as well, from line 13 of column 5, "The second comparator 401 compares the Cache-Tag to the CPU-Tag and compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407."

In response to Applicant's argument that the result of the error monitoring is used

to determine whether the fast hit or the slow hit path will be used, Examiner notes that Applicant has not claimed this per se. Rather, what is claimed is that "monitoring for errors in the stored tag address..." is performed, and that, subsequently, if a tag address error is detected, either "disregarding the first comparison..." or "utilizing results of the first comparison..." While it may be interpreted that this tag address error is the same result of monitoring for errors in the stored tag address, it need not be since it is not claimed in that way. Regardless, La Fetra discloses the subject matter as claimed in claim 1: a tag address error state results in a true hit and, otherwise, results in a fast hit (see above). Further, from the abstract, "A fast cache hit detection method and apparatus. The present invention provides a method and apparatus for quickly determining whether there is a cache hit in cache memory systems utilizing error corrected tags. The hit detection process is split into two paths. The first path includes a circuit to check and correct a tag stored in the cache memory. The second path tests the validity of the tag stored in the cache memory by computing the appropriate ECC information using memory address information supplied by the computer CPU and comparing the tag and ECC stored in the cache memory to the CPU address and computed ECC."

In response to Applicant's argument that generation of an ECC (e.g., ECC GEN 405) cannot read on the error monitoring of claim 1, it is not clear why Applicant has assigned 405 as the error monitor. Within element 401, La Fetra discloses ECC bits being compared. Within the true hit path, La Fetra shows, in parallel (contemporaneously), the operation of element 215, the tag check and correct circuit.

Both the ECC bits comparison operation and the tag check and correct circuit operation are at least contemporaneous to the tag comparison operation. Further, in response to Applicant's argument that the "'Tag check and correct circuit 215' of La Fetra does not make such a [tag address error] determination – rather the ECC generator 405 based on the generation of ECC and the comparison of ECCs are used", it is not clear where Applicant obtains this information. While it is true that 405 is used in generating ECC information, it is not until 401 that the ECC is actually compared.

In response to Applicant's argument regarding claim 2 that La Fetra does not teach using a single ECC in connection with a system that implements a fast and slow hit path, see above rejection. Further, two comprises one, although two may not comprise *only* one.

In response to Applicant's argument regarding claim 11 that Examiner identified the ECC generator 405 of La Fetra as teaching the error detector of claim 11, it is not clear how Applicant arrived at this conclusion. Examiner assigns such duties to the ECC bits comparing portion of 401.

In response to Applicant's argument regarding claim 11 that no such gating function coupled to La Fetra's second comparator 401 is described in La Fetra, Examiner contends that any such "gate" would be inherent in a computer logic system as described by La Fetra. From line 13 of column 5 (with emphasis), "The second comparator 401 compares the Cache-Tag to the CPU-Tag **and** compares the derived CPU-Tag ECC to the Cache-ECC. If both the Tags and the ECCs match, then the comparator 401 outputs a fast hit signal 407."

In response to Applicant's argument that the cited portion of La Fetra does not disclose claim 22's "means for coordinating timing between the first hit detection path means and the second hit detection path means", Examiner notes that disclosing "timing" need not be limited to the word "time" (or conjugations thereof). In the passage in question, Examiner has noted that the cache memory system "waits" for the true hit/miss signal. Any such waiting can only be accomplished through timing coordination means.

In response to Applicant's argument regarding claims 8 and 9 that La Fetra does not provide an error signal to an output gate based on detection of a tag error, from line 22 column 5 (with emphasis), "Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow. **If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.**" Wherein this being computer logic, a person of ordinary skill in the art at the time of the invention would have been motivated to pass the output through a "gate" of some kind, even if not explicitly disclosed as such, because a gate is an electronic switch that is the elementary component of a digital circuit that produces an electrical output signal that represents a binary 1 or 0 and is related to the states of one or more input signals by an operation of Boolean logic and La Fetra has disclosed that a tag error is detected (an input signal that represents a state) that results in the disallowance of a fast hit assertion (an electrical output signal that represents a binary 1 or 0).

In response to Applicant's argument that the output of the ECC generator 405 is not an error signal, Examiner has made no such assertion. Further, although Examiner has made no specific assertion as to what generates the error signal, such an error signal or error signal equivalent must exist in the system in order for the invention disclosed by La Fetra to operate (see above). Further, Applicant has made no claim as to what the error signal is generated by.

In response to Applicant's argument regarding claims 13 and 16 that La Fetra fails to provide a reasonable expectation of success in implementing latching means to coordinate timing, Examiner interprets this as a request to substantiate an official notice, which has been provided above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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